

CLAIM LISTING

No claims have been amended, canceled, or added. A Claim Listing is provided as a courtesy.

1. (Previously Presented) A method, comprising:

allocating an original percentage of bandwidth or number of accesses to memory by a memory controller; and

increasing the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller is less than the original percentage of bandwidth or number of accesses allocated to the memory controller; and

decreasing the bandwidth or number of accesses allocated to the memory controller to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the memory controller.

2. (Original) The method of claim 1, further comprising:

setting a window of time to monitor the percentage of bandwidth or number of accesses to memory by the memory controller; and

measuring the percentage of bandwidth used or number of accesses to memory by the memory controller during the window of time.

3. (Original) The method of claim 1, further comprising applying a mask to increase the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller.

4. (Original) The method of claim 1, further comprising applying a mask to decrease the

bandwidth or number of accesses allocated to the memory controller to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller.

5. (Previously Presented) An article of manufacture article of manufacture, comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations comprising,
allocating an original percentage of bandwidth or number of accesses to memory by a memory controller;

increasing the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller; and

decreasing the bandwidth or number of accesses allocated to the memory controller to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the memory controller.

6. (Original) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising:

setting a window of time to monitor the percentage of bandwidth or number of accesses to memory by the memory controller; and

measuring the percentage of bandwidth used or number of accesses to memory by the memory controller during the window of time.

7. (Original) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising applying a mask to increase the bandwidth or number of accesses allocated to the memory controller to a percentage higher than the original percentage of bandwidth or number of

accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller.

8. (Original) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising applying a mask to decrease the bandwidth or number of accesses allocated to the memory controller to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the memory controller are less than the original percentage of bandwidth or number of accesses allocated to the memory controller.

9. (Previously Presented) An apparatus, comprising:

a chipset having:

a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it; and

a memory controller to increase the percentage of memory bandwidth or the number of memory accesses allocated to the processor when the actual percentage of bandwidth or number of accesses to the memory by the processor is less than the original percentage of bandwidth or number of accesses allocated to the processor, the memory controller further to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the processor when the actual percentage of bandwidth or number of memory accesses by the processor is more than the original percentage of memory bandwidth or number of memory accesses allocated to the processor.

10. (Previously Presented) The apparatus of claim 9, further comprising:

a first register in the memory controller to set the percentage of memory bandwidth or the number of memory accesses allocated to the processor;

a second register in the memory controller to set a window of time to monitor percentage of memory bandwidth or number of memory accesses used by the processor; and

a counter in the memory controller to measure percentage of memory bandwidth used or number of memory accesses by the processor during the window of time.

11. (Previously Presented) The apparatus of claim 10, wherein the memory controller further comprises a mask to increase the percentage of memory bandwidth or the number of memory accesses allocated to the processor when memory accesses by the processor is less than the percentage of memory bandwidth or the number of memory accesses allocated to the processor.

12. (Previously Presented) The apparatus of claim 10, wherein the memory controller further comprises a mask to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the processor when memory accesses by the processor is more than the percentage of memory bandwidth or the number of memory accesses allocated to the processor.

13. (Previously Presented) The apparatus of claim 9, wherein the chipset further comprises:

a graphics memory having an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it; and

a graphics controller to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the graphics memory when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the graphics memory, the graphics controller further to decrease the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the graphics memory when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the graphics memory.

14. (Previously Presented) The apparatus of claim 13, wherein the chipset further comprises one or more input/output (I/O) devices, an individual I/O device having an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics controller to increase the percentage of graphics memory bandwidth or the

number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices, the graphics controller further to decrease the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices.

15. (Previously Presented) The apparatus of claim 13, wherein the processor further includes an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics controller to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor, the graphics controller further to decrease the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor.

16. (Previously Presented) The apparatus of claim 9, wherein the chipset further comprises a graphics memory having an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics memory to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to itself when an actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to itself, the graphics memory further to decrease the percentage of graphics memory bandwidth or the number of graphics memory

accesses allocated to itself when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to itself.

17. (Previously Presented) The apparatus of claim 16, wherein the chipset further comprises one or more input/output (I/O) devices, an individual I/O device having an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics memory to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices, the graphics memory further to decrease the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the one or more I/O devices when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the one or more I/O devices.

18. (Previously Presented) The apparatus of claim 16, wherein the processor further includes an original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to it, the graphics memory to increase the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when an actual percentage of graphics memory bandwidth or number of graphics memory accesses is less than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor, the graphics memory further to decrease the percentage of graphics memory bandwidth or the number of graphics memory accesses allocated to the processor when the actual percentage of graphics memory bandwidth or number of graphics memory accesses is more than the original percentage of graphics memory bandwidth or number of graphics memory accesses allocated to the processor.

19. (Previously Presented) The apparatus of claim 9, wherein the chipset further comprises one or more input/output (I/O) devices having an original percentage of memory bandwidth or number of memory accesses allocated to it, wherein the memory controller is to increase the percentage of memory bandwidth or the number of memory accesses allocated to the one or more I/O devices when an actual percentage of memory bandwidth or number of memory accesses by the one or more I/O devices is less than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices, the memory controller further to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the one or more I/O devices when the actual percentage of memory bandwidth or number of memory accesses by the one or more I/O devices is more than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices.

20. (Previously Presented) An apparatus, comprising:

a processor having an original percentage of memory bandwidth or number of memory accesses allocated to it, the processor having further a memory controller to increase the percentage of memory bandwidth or the number of memory accesses allocated to the processor when the actual percentage of bandwidth or number of accesses to the memory by the processor is less than the original percentage of bandwidth or number of accesses allocated to the processor, the memory controller further to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the processor when the actual percentage of bandwidth or number of memory accesses by the processor is more than the original percentage of memory bandwidth or number of memory accesses allocated to the processor.

21. (Previously Presented) The apparatus of claim 20, further comprising:

a first register in the memory controller to set the percentage of memory bandwidth or the number of memory accesses allocated to the processor;

a second register in the memory controller to set a window of time to monitor percentage of memory bandwidth or number of memory accesses used by the processor; and

a counter in the memory controller to measure percentage of memory bandwidth used or number of memory accesses by the processor during the window of time.

22. (Previously Presented) The apparatus of claim 20, wherein the memory controller further comprises a mask to increase the percentage of memory bandwidth or the number of memory accesses allocated to the processor when memory accesses by the processor is less than the percentage of memory bandwidth or the number of memory accesses allocated to the processor.

23. (Previously Presented) The apparatus of claim 20, wherein the memory controller further comprises a mask to decrease the percentage of memory bandwidth or the number of memory accesses allocated to the processor when memory accesses by the processor is more than the percentage of memory bandwidth or the number of memory accesses allocated to the processor.

24. (Previously Presented) A method, comprising:

allocating to a processor an original percentage of memory bandwidth or number of memory accesses;

increasing the memory bandwidth or number of memory accesses allocated to the processor to a percentage higher than the original percentage of memory bandwidth or number of memory accesses allocated to the processor when actual accesses to memory by the processor is less than the original percentage of memory bandwidth or number of memory accesses allocated to the processor; and

decreasing the bandwidth or number of accesses allocated to the processor to a percentage lower than an original memory bandwidth or number of memory accesses allocated to the processor when actual accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the processor.

25. (Previously Presented) The method of claim 24, further comprising:

setting a window of time to monitor the percentage of bandwidth or number of

accesses to memory by the processor; and

measuring the percentage of bandwidth used or number of accesses to memory by the processor during the window of time.

26. (Previously Presented) The method of claim 25, further comprising applying a mask to increase the bandwidth or number of accesses allocated to the processor to a percentage higher than the original percentage of bandwidth or number of accesses allocated when accesses to memory by the processor are less than the original percentage of bandwidth or number of accesses allocated to the processor.

27. (Previously Presented) The method of claim 25, further comprising applying a mask to decrease the bandwidth or number of accesses allocated to the processor to a percentage lower than an original bandwidth or number of accesses allocated when accesses to memory by the processor are less than the original percentage of bandwidth or number of accesses allocated to the processor .

28. (Previously Presented) The apparatus of claim 24, further comprising:

allocating to a graphics controller an original percentage of memory bandwidth or number of memory accesses;

increasing the memory bandwidth or number of memory accesses allocated to the graphics controller to a percentage higher than the original percentage of memory bandwidth or number of memory accesses allocated to the graphics controller when actual accesses to memory by the graphics controller is less than the original percentage of memory bandwidth or number of memory accesses allocated to the graphics controller; and

decreasing the bandwidth or number of accesses allocated to the graphics controller to a percentage lower than an original memory bandwidth or number of memory accesses allocated to the graphics controller when actual accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the graphics controller.

29. (Previously Presented) The apparatus of claim 24, further comprising:

allocating to one or more input/output (I/O) devices an original percentage of memory bandwidth or number of memory accesses;

increasing the memory bandwidth or number of memory accesses allocated to the one or more I/O devices to a percentage higher than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices when actual accesses to memory by the one or more I/O devices is less than the original percentage of memory bandwidth or number of memory accesses allocated to the one or more I/O devices; and

decreasing the bandwidth or number of accesses allocated to the one or more I/O devices to a percentage lower than an original memory bandwidth or number of memory accesses allocated to the one or more I/O devices when actual accesses to memory by the memory controller are more than the original percentage of bandwidth or number of accesses allocated to the one or more I/O devices.